REMARKS

Applicant thanks the examiner for their detailed review.

Claim Rejections -35 USC § 112

The Office Action states:

> **Claims 31-33** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 31 has been amended to remove reference to the I/O hub and replace the first reference to "a controller hub."

Claim Rejections -35 USC § 102(b)

The Office Action States:

> 5. **Claims 1-4, 10-15, 21-25, 30, and 34-35,** are rejected under 35 U.S.C. 102(e) as being anticipated by Scarpino (US pat. 6,748,496).

"[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention …" MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim*." *Richardson v., Suzuki Motor Co*., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Applicant's amended claim 1 includes, "transmitting a write completion signal corresponding to each of the plurality of write transactions with the controller hub to the requesting device in response to buffering data associated with each of the plurality of write transactions; and flushing the data associated with the plurality of transactions in the buffer as write combined data to an I/O device in response to receiving a flush signal from the requesting device after transmitting

the write completion signal corresponding to each of the plurality of write transactions."

Applicant respectfully submits that Scarpino does not disclose transmitting a write completion signal for each write transaction or flushing the data in response to receiving a flush signal. Instead, Scarpino discloses performing a burst of data from the write collecting buffer **52** with the buffer is filled (See col. 5 lines 49-52). The only mention of a flush signal is in col. 6 lines 1-4, when Scarpino describes flushing a cache line from a cache in a processor, not flushing data held in a buffer within a controller hub in response to a flush signal from a requesting device, as in applicant's claim 1. Furthermore, as described below Graham also does not disclose transmitting write completion signals and flushing data in response to receiving a flush signal from a requesting device (See the discussion under the 103 rejections regarding Graham).

Applicant's claim 12 includes, "the first and the second write transactions to reference **partial data of a cache line** within the processor, wherein the first and second write transactions include **a write combinable attribute** to indicate the first and the second partial write transactions as write combinable," (claim 12 with emphasis).

First, applicant respectfully submits that Scarpino does not disclose an attribute included in a transaction to indicate the transaction is write combinable. The Office Action cites Scarpino's use of a specific condition in col. 5; however, the specific condition Scarpino discloses is that the "address of the write falls within a pre-configured range of address and the range of addresses is not cache by either L1 cache," (col. 5 lines 8-10) (See also col. 6 lines 12-16). Therefore, Scarpino requires address range logic in the bridge to detect whether the write address is within an appropriate pre-configured range. In contrast, applicant includes an attribute within the transaction to indicate it is write combinable.

Second, applicant respectfully submits that Scarpino does not disclose the capability of writes, which are combined by write combining buffer 52, are partial data writes. Instead, the only

mention of data length in reference to buffer 52 is that it has longer cache lines capable of storing more data than a cache line of L1 cache 62 (See col. 4 lines 501-54). Furthermore, in the discussion of limitations of buffer 52, Scarpino states that the address range for the specified range of write-combinable addresses is un-cacheable (See col. 6 lines16-17), i.e. not partial writes to a cache line as in applicant's claim 12.

Applicant's claim 21 includes, "a write combining module to store first data associated with the first combinable write transaction in the buffer and send a first write completion signal to the first device in response to storing the first data in the buffer, store second data associated with the second combinable write transaction in the buffer and send a second write completion signal to the first device in response to storing the second data in the buffer, and flush the first data and the second data as combined data to the second device in response to receiving a flush signal from the first device." As stated above in reference to claim 1, Scarpino does not disclose sending a write completion for each write combinable transaction back to the first device, as applicant's claim 21. Furthermore, Scarpino does not disclose flushing in response to a flush signal from the first device as in applicant's claim 21, but rather buffer 52 of Scarpino writing all data when it fills with a predetermined number of bytes of data.

Applicant's claim 34 includes, "protocol logic to transmit a flush signal to the hub to initiate a flush of data associated with the plurality of write transactions in response to detecting a flush event and receiving, with the receiving logic, a last write completion for a last write transaction of the plurality of write transactions." As stated above, Scarpino's buffer 52 only writes all of the data after the buffer is filled with a predetermined number of bytes of data; therefore, there is no disclosure of a processor that includes protocol logic, which sends a flush signal both in response to receiving a last write completion signal and detecting a flush event, as in applicant's claim 34.

Claim Rejections -35 USC § 103(a)

The Office Actions states:

18. **Claims 5-9, 16-19, 26-29, 31-33, and 36**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Scarpino (US pat. 6,748,496) in view of Graham et al. (US pat. 6,233,641).

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

Applicant's claim 31 includes, "determining whether a latency condition exists, the latency condition including at least a delay in receiving a next combinable write transaction from the processor," (claim 31). The Office Action states that Scarpino fails to disclose determining if a latency condition exists, flushing the data in response to the latency condition existing, and sending a write completion signal for each of the plurality of writes.

Applicant respectfully submits that Graham only discloses a general delayed operation including an acknowledgment, not detecting a latency condition between a **next combinable write transaction**, such as in applicant's claim 31. Note that Graham merely describes the general form of a delayed operation (receive a command that operation has been executed) and a posted operation (no status acknowledgment). However, there is no determining if a latency condition exists before flushing data in Graham, as in applications claim 31. Instead, in Graham a master

issues a delayed operation, allows the operation to be performed, and then receives an acknowledgement/status command. Here, if the Office Action analogizes each of applicant's write combinable operations as equivalent to Graham's delayed operations, and applicant's write completions as acknowledgements, the difference can be seen in that Graham does not disclose detecting any latency event between **a next delayed operation**, or in this example of applicant's claim a latency event between a last write combinable transaction of the plurality of write combinable transactions and a next combinable write transaction, as in applicant's claim 31.

Similarly, applicant's new claim 37 includes, "latency detection logic to detect occurrence of a latency condition, the latency condition including at least a delay in receiving a next combinable write transaction from the processor."

Conclusion

Therefore, Applicants respectfully submit that claims 1, 12, 21, 31, 34, and 37, as well as their dependent claims, are in condition for allowance for at least the same reasons stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a another telephone interview would in any way expedite the prosecution of the present application , the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
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Dated: June 4, 2009

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